REMARKS

Claims 21-36 remain in this application. Claims 1-20 are cancelled. New claims 21-36 are added.

Applicants thank the Examiner for the detailed study of the application and prior art. Applicants have cancelled all existing independent and dependent claims and substituted new claims 21-36 with independent claims 21 and 28. Applicants contend that the new claims are patentable over the cited prior art, and more particularly, the cited U.S. Patent No. 5,585,763 to Navabi et al. (hereinafter "Navabi") used to reject now cancelled claims 1 and 4-16.

Applicants file a Request for Continued Examination (RCE) in this After Final Amendment to have new claims 21-36 considered by the Examiner.

The two independent claims 21 and 28 now recite the amplifier driver that includes a first operational amplifier having first and second differential polarity inputs, the inverting level shifter, the complimentary first and second output transistor circuits and first and second current mirror circuits that form the current mirror node and output node. At a no-load condition, the voltage at the current mirror node and voltage at the output node are substantially the same.

A current feedback circuit extends from the current mirror node to an input of the first operational amplifier. A feedback operational amplifier is positioned within the current feedback circuit and has an output and a first input operatively connected to the output node and a second input operatively connected to the current mirror node. First and second auxiliary bias current source circuits and first and second current mirror circuits are operatively connected to

the output of the feedback operational amplifier such that the current mirror node substantially tracks the output voltage at the output current node and substantially removes current mirror distortion for different values of load resistance.

FIG. 8 is an example of the circuit represented by new claim 21.

As noted in claim 28, the second current mirror circuit and second auxiliary bias current source can be operatively connected to an input of the operational amplifier as shown in FIG. 8. The second auxiliary bias current source is operatively connected to an inverting input of the first operational amplifier and the auxiliary bias current source circuit can be referenced to ground.

Other details as shown in FIG. 8 include the current feedback circuit connected to an inverting input of the first operational amplifier and a resistor circuit within the current feedback circuit. This current feedback circuit could have two paths. The first input of the feedback operational amplifier is formed as a non-inverting input and the current feedback circuit can be connected thereto. A feedback transistor can be operatively connected to the output of the feedback operational amplifier and formed as a MOSFET with a source-drain path coupled to voltage rails through the first auxiliary bias current source circuit.

Navabi discloses an operational amplifier and a complimentary pair of transistors 345, 347, 355, 357, and a pair of error amplifiers 370, 375. Nowhere does Navabi suggest first and second current mirror circuits forming a current mirror node and first and second output transistor circuits forming an output node such that the voltages are

substantially the same at a no-load condition, and a current feedback circuit that includes a feedback operational amplifier and a first input connected to the output node and second input connected to the current mirror node, and first and second auxiliary bias current source circuits and first and second current mirror circuits operatively connected to the output of the feedback operational amplifier such that the current mirror node substantially tracks the output voltage at the output current node and substantially removes current mirror distortion for different values of load resistance.

Although the intersection of various circuit components and lines such as at 343 and 353 and 344 and 354 in Navabi may suggest nodes, nowhere does Navabi suggest the circuit structure and function as presented in this Amendment.

Applicants contend that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due.

If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **MAIL STOP AF, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450,** on this 11th day of April, 2006.

Julie Lalan